In re Patent Application of
COFLER ET AL.
Serial No. 10/082,816
Filed: FEBRUARY 25, 2002

REMARKS

Applicants thank the Examiner for the careful and thorough examination of the present application, and for the indication of allowable subject matter. By this amendment, the specification has been amended to eliminate minor informalities contained therein. Claims 25-50 remain pending in the application. Favorable reconsideration is respectfully requested.

I. The Invention

As shown in FIGS. 1 and 2, for example, the disclosed invention is directed to a method of handling branching instructions within a processor. The present mechanism for handling branching instructions allows an overall improvement in the branching latency, and applies particularly to a processor including decoupled architecture. According to the invention, with the processor core being clocked by a clock signal, a branching instruction received by the central unit in the course of a current cycle of the clock signal is processed (i.e. executed) in the course of the current cycle. Thus, the branching module is transferred into the central unit, which makes it possible to process the branching instructions much more rapidly.

II. The Claims are Patentable

Claims 25-27, 30, 36-40 and 50 were rejected in view of Emma et al. (U.S. 5,353,421) taken alone or in combination with European Patent Application No. 1050805 for the reasons

set forth on pages 3-11 of the Office Action. Claims 28, 29, 31-35 and 41-49 were indicated as being directed to allowable subject matter. Applicants contend that Claims 25-27, 30, 36-40 and 50 clearly define over the cited references, and in view of the following remarks, favorable reconsideration of the rejections under 35 U.S.C. §102 and §103 is requested.

Independent method Claims 25 and 36 each set forth that a branching instruction received in the course of a current cycle of the clock signal is processed in the course of the current cycle. Independent processor Claim 38 includes a central unit for issuing instructions to the processing units based upon corresponding program instructions, and including a branching module for receiving a branching instruction during a current clock cycle, and processing this branching instruction during the current clock cycle.

It is these combinations of features which are not fairly taught or suggested in the cited references and which patentably define over the cited references.

The Examiner has relied on the Emma et al. patent as allegedly disclosing a pipelined architecture that "will process a branching instruction immediately without wait when the instruction is received" while referring to Fig. 1 of the Emma et al. patent. Furthermore, the Examiner asserts that the system of Emma et al. includes a central unit for issuing instructions to the processing units based upon corresponding program instructions, and including a branching module for receiving a branching instruction during a current clock cycle, and processing this branching instruction during the

current clock cycle. The Examiner refers to Figs. 10 and 12, and instruction buffer 11 to support his position.

The Emma et al. patent is directed to a multi-prediction branch prediction mechanism that predicts each conditional branch at least twice, first during the instruction-fetch phase of the pipeline and then again during the decode phase of the pipeline. The mechanism uses at least two different branch prediction mechanisms. The reference discusses "cycles" of the pipeline (e.g. column 1 and column 7) and specifically teaches, at column 5, lines 29-32, that "the BHT makes its prediction during the instruction-fetch phase of the pipeline and that it can be several cycles until the branch instructions is finally executed."

Accordingly, the Examiner is mischaracterizing the actual teachings of the Emma et al. reference as there is no suggestion that a branching instruction, received by the central unit in the course of a current cycle of the clock signal, is processed during the current cycle, as claimed.

As the Examiner is aware, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. The identical invention must be shown in as complete detail as is contained in the claim.

The European patent application was cited to teach the use of a guard-indication register. Without discussing the details thereof, it is sufficient to note that nothing in such reference discusses a branching instruction, received by the central unit in the course of a current cycle of the clock

signal, is processed during the current cycle, as claimed. As such, this reference cannot make up for the deficiencies of the Emma et al. reference as discussed above.

There is simply no teaching or suggestion in the cited references to provide the combination of features as claimed. Accordingly, for at least the reasons given above, Applicants maintain that the cited references do not disclose or fairly suggest the invention as set forth in Claims 25, 36 and 38. Furthermore, no proper modification of the teachings of these references could result in the invention as claimed. Thus, the rejections under 35 U.S.C. §102(e) and §103(a) should be withdrawn.

It is submitted that the independent claims are patentable over the prior art. In view of the patentability of the independent claims, it is submitted that their dependent claims, which recite yet further distinguishing features are also patentable over the cited references for at least the reasons set forth above. Accordingly, these dependent claims require no further discussion herein.

III. Conclusion

In view of the foregoing remarks, it is respectfully submitted that the present application is in condition for allowance. An early notice thereof is earnestly solicited. If, after reviewing this Response, there are any remaining informalities which need to be resolved before the application can be passed to issue, the Examiner is invited and

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respectfully requested to contact the undersigned by telephone in order to resolve such informalities.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number 703-872-9306 to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 this 10th day of February, 2005.